What is claimed is:

1. A management port for a wireless device platform, comprising:

a communication link to be used in inter-processor communication for the wireless device platform, the communication link to provide an inbound link and an outbound link, and to control data flow over the inbound and outbound links; and

a management block to receive command data through a predetermined logic channel in the inbound link and generate a corresponding command signal on a microprocessor bus system that is local to the command link to perform a management function for the microprocessor system, the management block being further adapted to receive a response signal from the bus and transmit corresponding response data through a predetermined logic channel in the outbound link.

2. The management port of claim 1, wherein the communication link includes a physical layer to provide both the inbound and outbound links with multiple logic channels, and a data link protocol to control data flow over the inbound and output links.

3. The management port of claim 1, wherein the management function includes a debug function.

4. The management port of claim 1, wherein the management function includes accessing memory.

5. The management port of claim 1, wherein the management function includes accessing configuration registers.

6. The management port of claim 1, wherein the management function includes accessing a peripheral device of the microprocessor system.

7. The management port of claim 1, wherein the management block includes:

a command register connected to the bus and to the communication link, the command register to temporarily store the command data delivered through the predetermined logic channel in the inbound link;

a response register connected to the bus and to the communication link, the response register to temporarily store response data from the bus; and

a manageability controller connected to the microprocessor bus, the command register, and the response register, the manageability controller being adapted to determine when command data is received at the command register and to transmit the corresponding command signal over the bus, and further being adapted to receive the response signal from the bus and store corresponding response data at the response register, and to transmit the response data through the predetermined logic channel in the outbound link.

8. A microprocessor system, comprising:

a processor core;

at least one processor subsystem to communicate with the processor core using at least one bus;

a communication link connected to the at least one bus to enable inter-processor communication, the communication link to provide a multi-channel inbound link and a multi-channel outbound link, and to control data flow over a plurality of channels for both the inbound and outbound links; and

a management block to receive command data using a predetermined logic channel in the inbound link and generate a corresponding command signal on the at least one bus to perform a management function for at least one of the processor core and the at least one processor subsystem, the management block being further adapted to receive a response signal from the bus and transmit corresponding response data through a predetermined logic channel in the outbound link.

9. The microprocessor system of claim 8, wherein the management function includes a debug function.

10. The microprocessor system of claim 8, wherein the at least one processor subsystem includes a memory controller.

11. The microprocessor system of claim 8, wherein the at least one processor subsystem includes configuration registers.

12. The microprocessor system of claim 8, wherein the at least one processor subsystem includes a security module.

13. The microprocessor system of claim 8, wherein the at least one processor subsystem includes a Universal Serial Bus (USB) client.

14. The microprocessor system of claim 8, further comprising a peripheral device, the management block being adapted to generate the corresponding command signal on the at least one bus to perform a management function for the at least one peripheral device.

15. A microprocessor system for a wireless device, comprising:

a processor core and at least one processor subsystem;

at least one bus to connect the processor core to the at least one processor subsystem;

means for providing a multi-channel inbound link and a multi-channel outbound link for inter-processor communication in the wireless device, and to control data flow over a plurality of channels for both the inbound and outbound links;

means for receiving command data through a predetermined logic channel in the inbound link and generating a corresponding command signal on the bus with an

appropriate communication protocol to perform a management function for at least one processor subsystem; and

means for receiving a response signal from the bus and transmitting corresponding response data through a predetermined logic channel in the outbound link.

16. The microprocessor system of claim 15, wherein the means for receiving command data through a predetermined logic channel in the inbound link and generating a corresponding command signal on the bus to perform a management function for at least one processor subsystem and the means for receiving a response signal from the bus and transmitting corresponding response data through a predetermined logic channel in the outbound, includes a management block comprising:

a command register connected to the bus, the command register to temporarily store the command data delivered through the predetermined logic channel in the inbound link;

a response register connected to the bus, the response register to temporarily store response data from the bus; and

a manageability controller connected to the bus, the command register, and the response register, the manageability controller being adapted to determine when the command data is received at the command register and to transmit the corresponding command signal over the bus, and further being adapted to receive the response signal from the bus and store the corresponding response data at the response register, and to transmit the response data through the predetermined logic channel in the outbound link.

17. The microprocessor system of claim 15, wherein the means for providing a multi-channel inbound link and a multi-channel outbound link for inter-processor communication in the wireless device includes means to provide a plurality of

channels to communicate with an embedded communications microprocessor system.

18. The microprocessor system of claim 17, wherein the embedded communications microprocessor system is adapted to wirelessly communicate with at least one other devices.

19. A system, comprising:

an embedded applications microprocessor system and an embedded communications microprocessor system, each microprocessor system including a communication link to enable inter-processor communication over multiple channels;

a substantially omni-directional antenna connected to the embedded communications microprocessor system;

an inter-processor communication bus connected to the communication links of both the applications microprocessor system and the communications microprocessor system; and

the communications link of the applications microprocessor system including a manageability port to allow the communications microprocessor system to access a microprocessor bus for the applications microprocessor system using at least one predetermined channel and to perform management functions in the applications microprocessor system.

20. The system of claim 19, wherein:

the communications link includes a multi-channel inbound link and a multi-channel outbound link, the communications link being adapted to control data flow over the inbound and outbound links; and

the manageability port is adapted to receive command data through a predetermined logic channel in the inbound link and generate a corresponding command signal on the microprocessor bus, and further is adapted to receive a

response signal from the bus and transmit corresponding response data through a predetermined logic channel in the outbound link.

21. The system of claim 20, wherein the embedded communications microprocessor system includes a microprocessor system adapted to wirelessly communicate with at least one other device.

22. The system of claim 21, wherein the microprocessor system is adapted to wirelessly communicate with at least one other devices using IEEE 802.11 technology.

23. The system of claim 21, wherein the microprocessor system is adapted to wirelessly communicate with at least one other device using cellular radio technology.

24. The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using general packet radio service (GPRS) technology.

25. The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using code division multiple access (CDMA) technology.

26. The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using wideband code division multiple access (WCDMA) technology.

27. The system of claim 19, the embedded communications microprocessor system includes:

a microprocessor system adapted to wirelessly communicate with at least one other devices using an IEEE 802.11 technology; and

a microprocessor system adapted to wirelessly communicate with at least one other device using cellular radio technology.

28. A method, comprising:

receiving an inter-processor communication signal at a communications link for a microprocessor system, the communication link to provide a multi-channel inbound link and a multi-channel outbound link for the microprocessor system, and to control inter-processor data flow over the inbound and outbound links, wherein receiving an inter-processor communication signal includes receiving a signal using a predetermined channel of the inbound link, the signal including command data to perform a management function for a microprocessor subsystem; and

processing the command data to transmit a corresponding command signal on a microprocessor bus using an appropriate bus communication protocol to perform the management function.

29. The method of claim 28, further comprising:

processing a response signal received over the microprocessor bus from the microprocessor subsystem into a response data; and

transmitting a signal that includes the response data using a predetermined channel of the outbound link.

30. The method of claim 29, wherein:

processing the command data includes

routing the command data through a command register in preparation to transmit the corresponding command signal on the microprocessor bus; and

processing a response signal received over the microprocessor bus from the microprocessor subsystem into response data includes routing the response data through a response register in preparation to transmit the signal that includes the response data using the predetermined channel on the outbound link.